FIG. 1

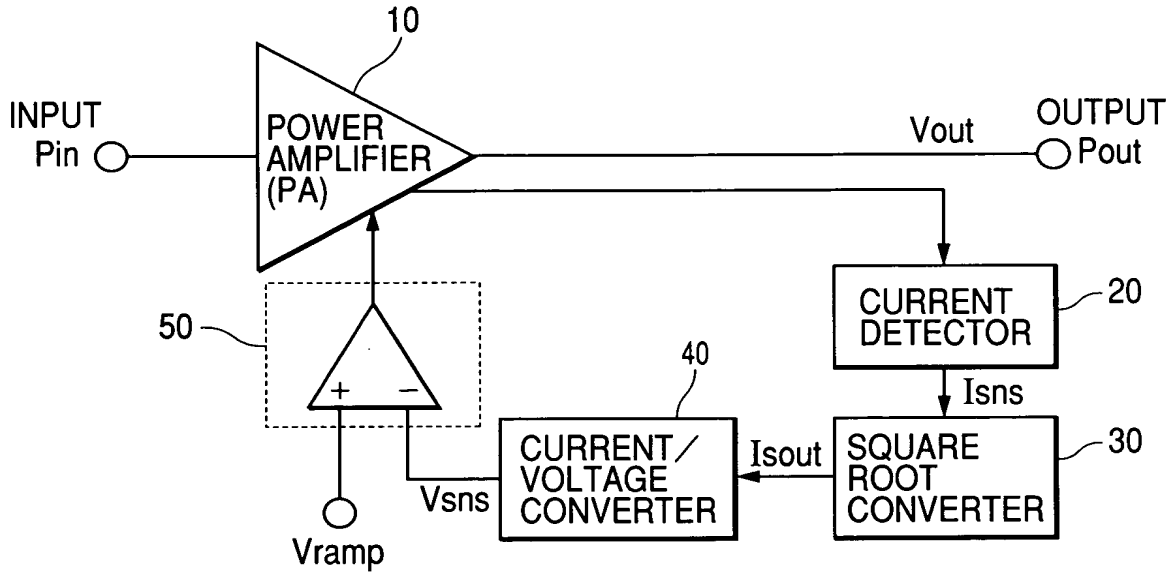

10
INPUT
Pin
POWER
AMPLIFIER
(PA)
Vout
OUTPUT
Pout
CURRENT
DETECTOR
20
50
40
Isns
CURRENT/
VOLTAGE
CONVERTER
Isout
SQUARE
ROOT
CONVERTER
30
Vsns
Vramp

FIG. 2

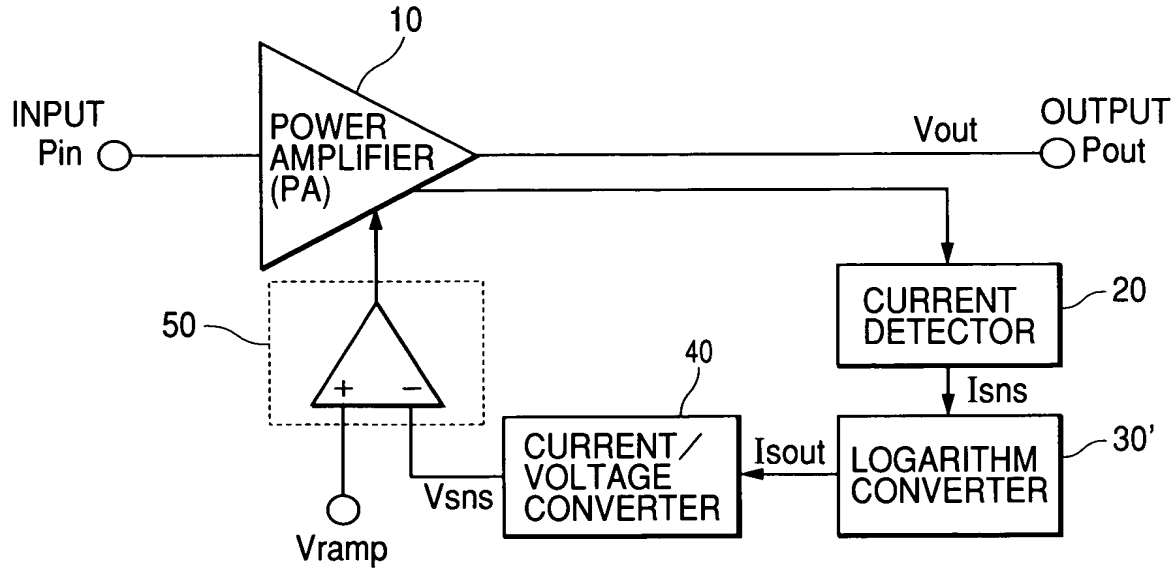

10
INPUT
Pin
POWER
AMPLIFIER
(PA)
Vout
OUTPUT
Pout
CURRENT
DETECTOR
20
50
40
Isns
CURRENT/
VOLTAGE
CONVERTER
Isout
LOGARITHM
CONVERTER
30'
Vsns
Vramp

FIG. 3

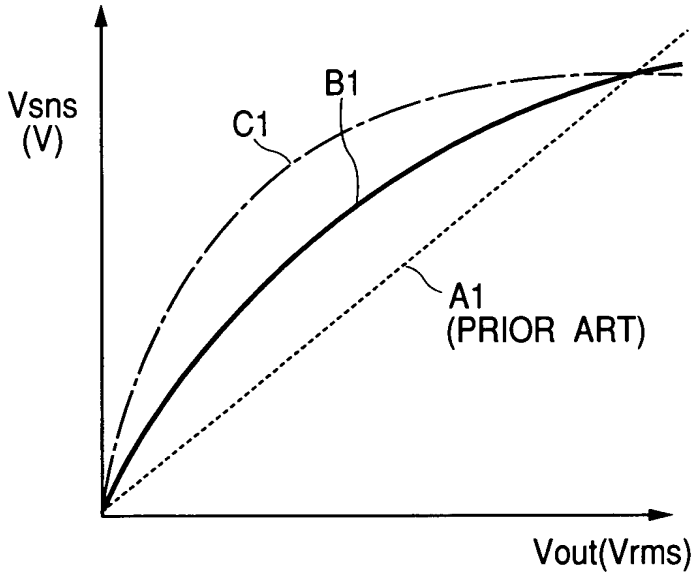

Vsns
(V)
B1
C1
A1
(PRIOR ART)
Vout(Vrms)

FIG. 4

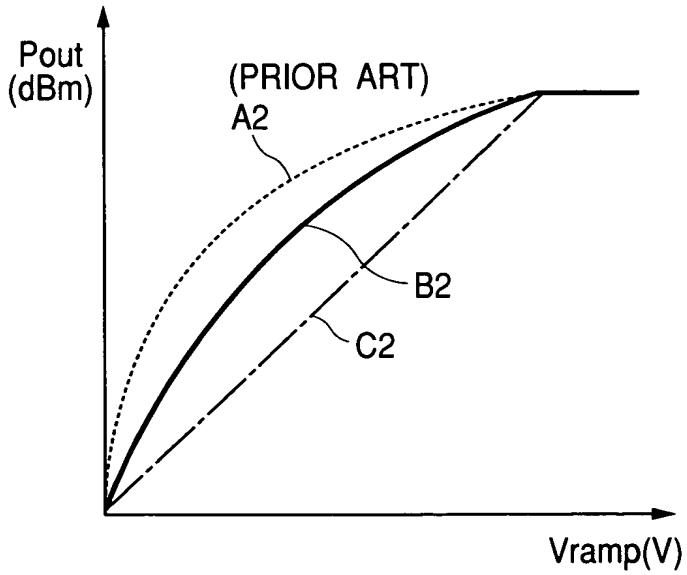

Pout
(dBm)
(PRIOR ART)
A2
B2
C2
Vramp(V)

FIG. 5

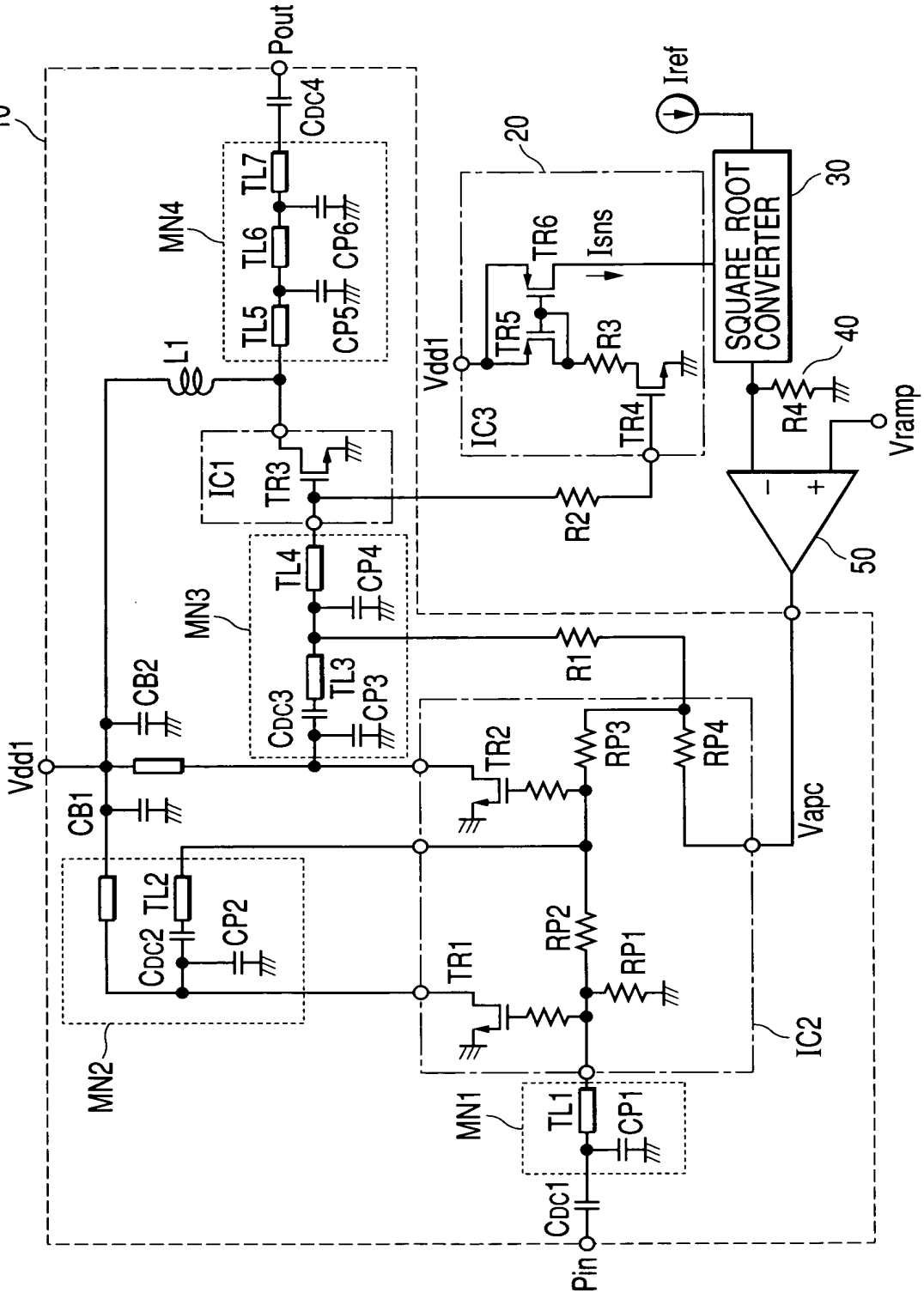

10
Pout
CDC4
MN4
TL7
TL6
TL5
CP6
CP5
L1
IC1
TR3
TL4
CP4
MN3
CDC3
TL3
CP3
CB2
CB1
Vdd1
CDC2
TL2
CP2
MN2
TR2
RP3
RP4
Vapc
TR1
RP2
RP1
IC2
MN1
TL1
CP1
CDC1
Pin
20
Iref
TR6
Isns
TR5
R3
Vdd1
IC3
TR4
R2
SQUARE ROOT CONVERTER
30
40
R4
Vramp
50

FIG. 6

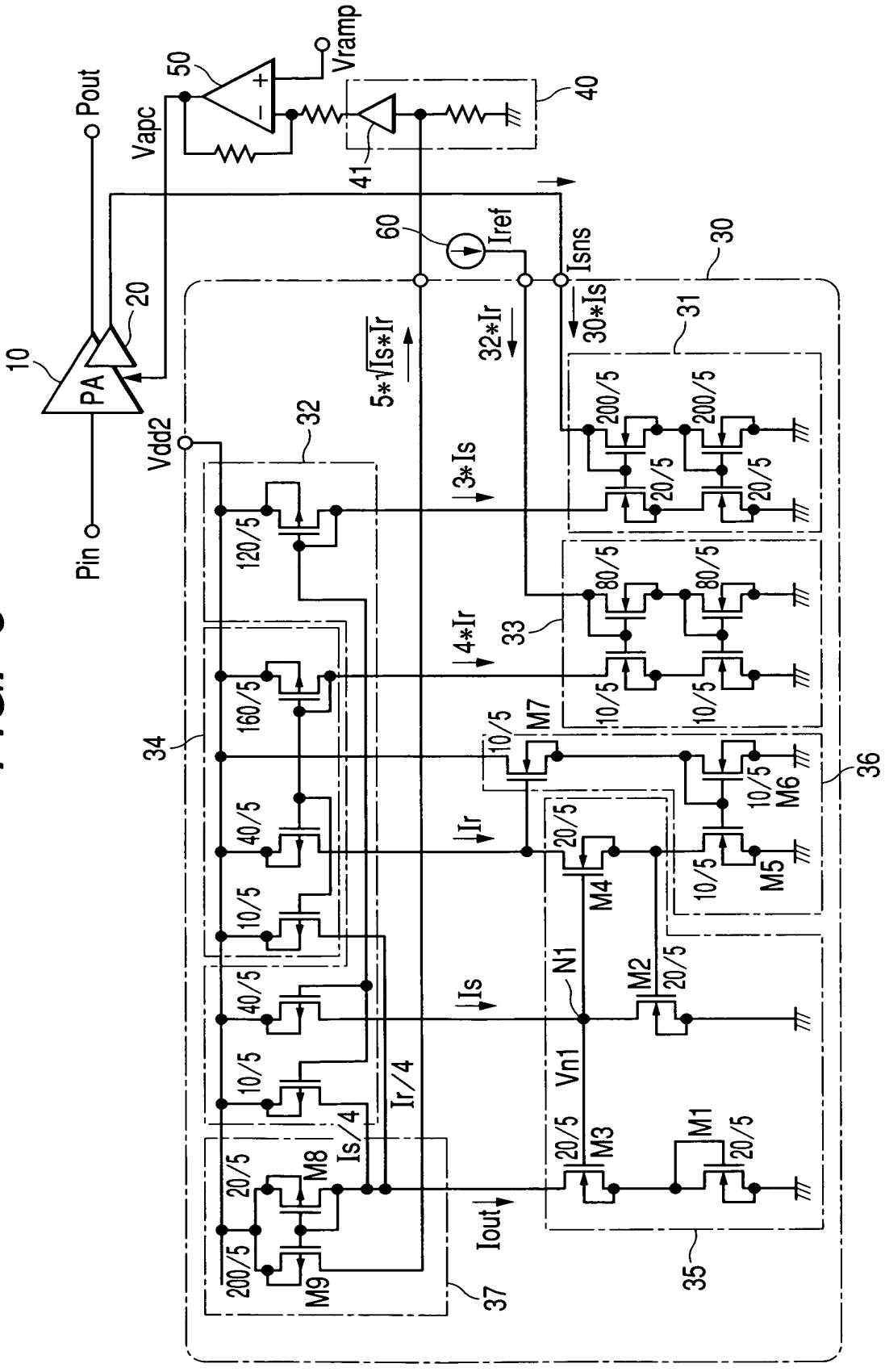

Pout
Vapc
50
Vramp
40
41
60
Iref
Isns
30
10
PA
20
Pin
Vdd2
32
5*√Is*Ir
32*Ir
30*Is
31
3*Is
4*Ir
33
34
Ir
Is
Ir/4
Is/4
N1
Vn1
M1
M2
M3
M4
M5
M6
M7
M8
M9
Iout
35
36
37
120/5
160/5
40/5
10/5
20/5
200/5
80/5

FIG. 7

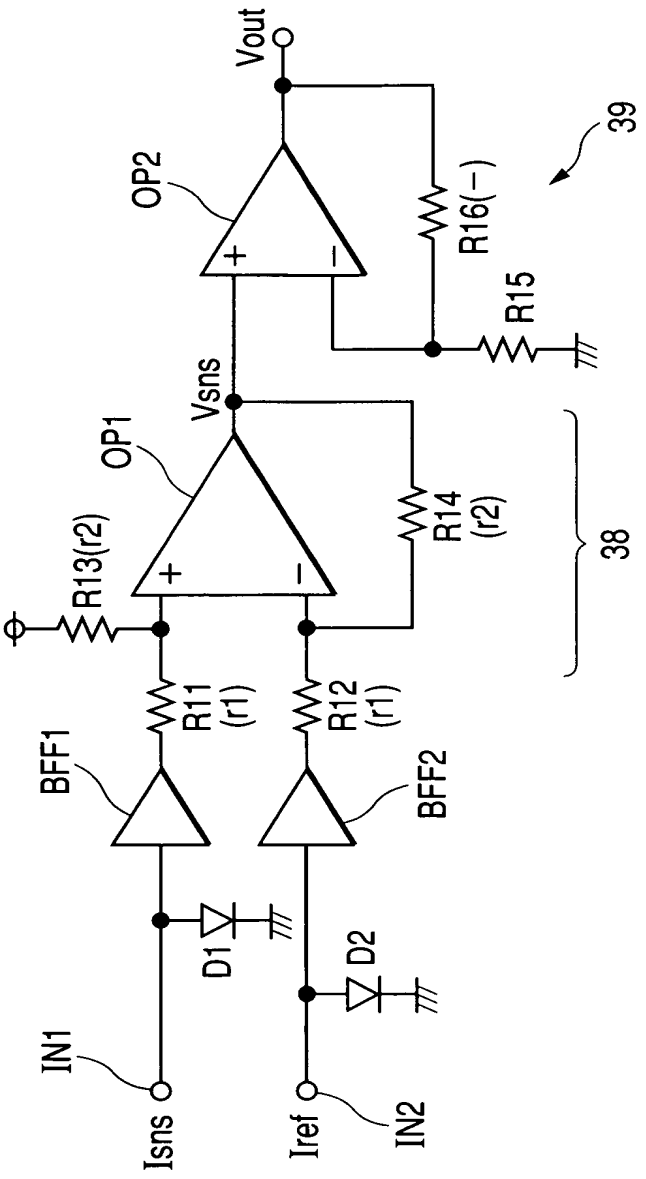

Vout
OP2
R16(−)
R15
39
Vsns
OP1
R14
(r2)
38
R13(r2)
R11
(r1)
R12
(r1)
BFF1
BFF2
D1
D2
IN1
Isns
Iref
IN2

FIG. 8

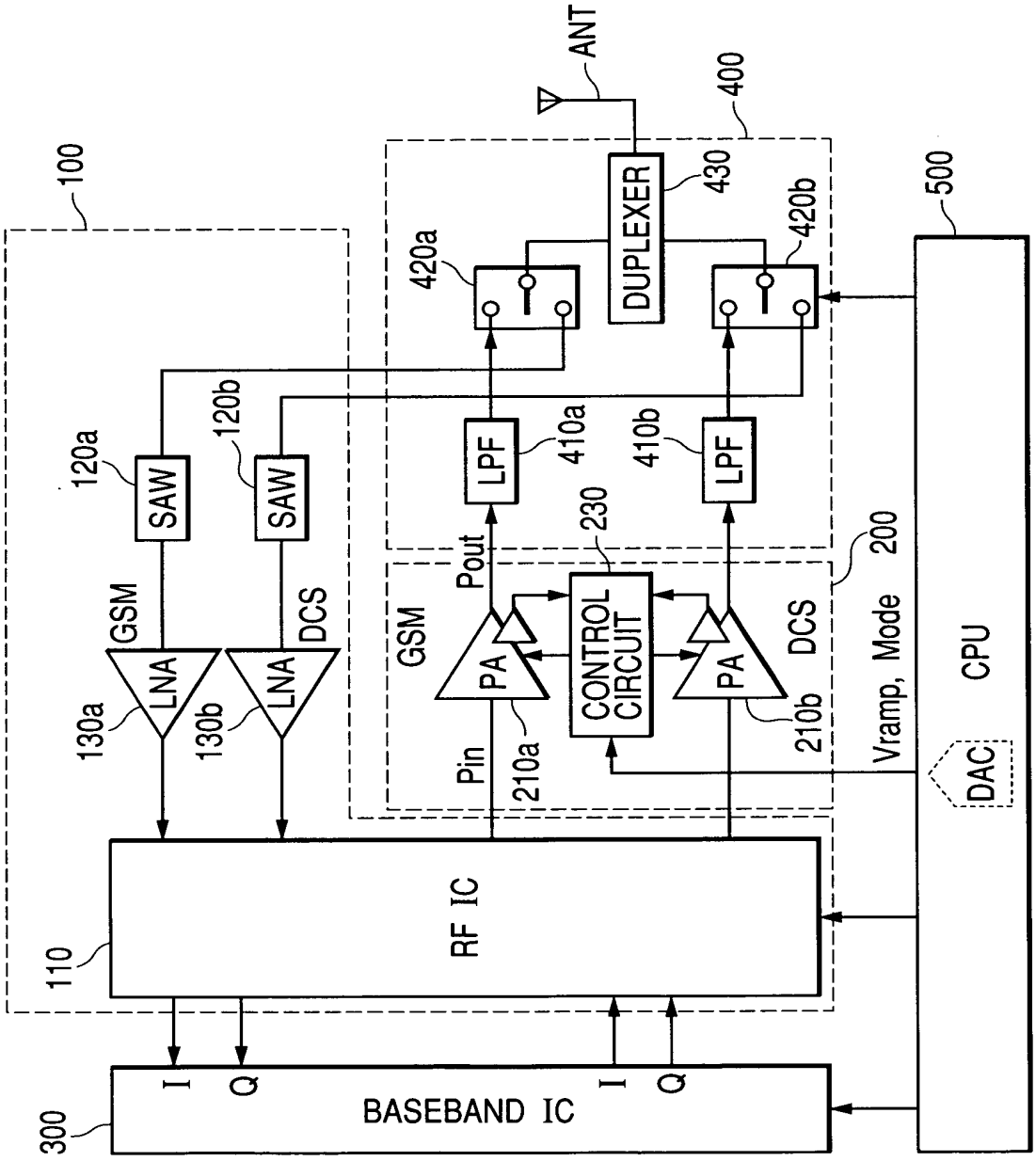
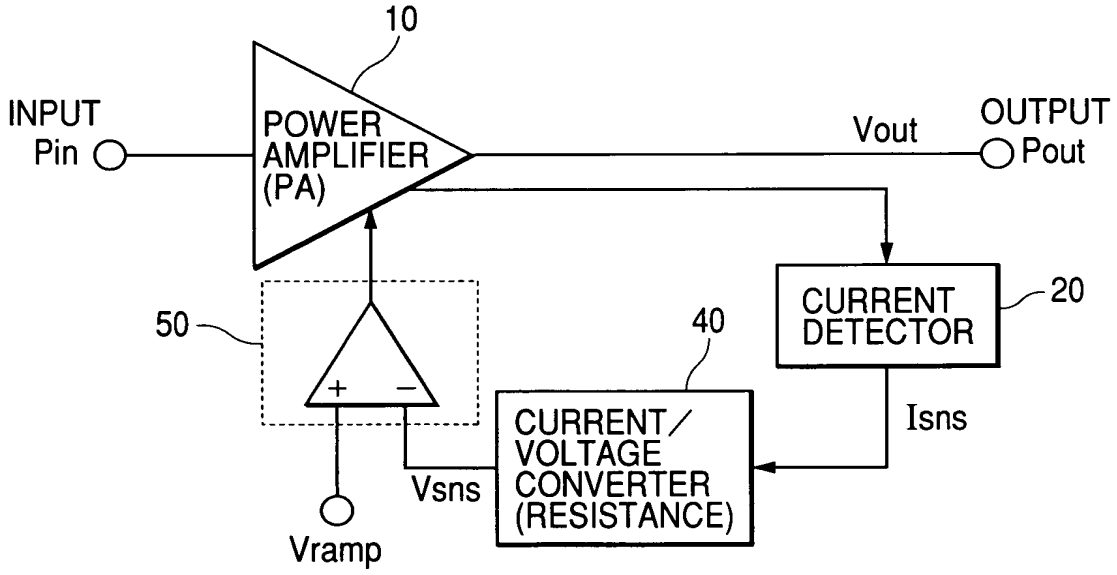

ANT
400
100
500
DUPLEXER
430
420a
420b
120a
120b
SAW
SAW
LPF
LPF
410a
410b
230
200
GSM
DCS
Pout
Pin
PA
PA
CONTROL CIRCUIT
130a
130b
LNA
LNA
210a
210b
Vramp, Mode
CPU
DAC
RF IC
110
I
Q
I
Q
BASEBAND IC
300

FIG. 9


10
INPUT
Pin
POWER
AMPLIFIER
(PA)
Vout
OUTPUT
Pout
CURRENT
DETECTOR
20
50
40
+
−
CURRENT/
VOLTAGE
CONVERTER
(RESISTANCE)
Isns
Vsns
Vramp